H-706-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	09/864,338	Confirmation No. 3538
Applicant	:	J. ETOH et al.	
Filed	:	May 25, 2001	
Title	:	LARGE SCALE INTEGRATED CIRCUIT WITH SENSE AMPLIFIER CIRCUITS FOR LOW VOLTAGE OPERATION	
TC/AU	:	2827	
Examiner	:	S. L. Mai	
Customer No.	:	24956	

SUPPLEMENTAL DECLARATION
FOR REISSUE PATENT APPLICATION

MAIL STOP: Reissue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

As a below named inventor, I hereby declare that:

My citizenship, residence and post office address are as stated next to my name.

Kiyoo Itoh

Citizenship: Japan

Residence: Higashikurume, Japan

Post Office Address:

c/o Hitachi, Ltd. of Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo, JAPAN,

Yoshinobu Nakagome

Citizenship: Japan

Residence: Hachioji, Japan

Post Office Address:

c/o Hitachi, Ltd. of Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo, JAPAN,

I believe I am the original, first and joint inventor of the invention described and claimed in U.S. Letters Patent No. 5,526,313 and in the specification of the foregoing reissue application and for which improvement is solicited a reissue patent.

IDENTIFICATION OF ERROR

The patentees had a right to claim all aspects of the invention. There is an error in that the patentees claimed less than they had a right to claim in the patent. Specifically, the patentees had a right to claim the embodiments of the invention shown in Figs. 12A-15C.

To correct the error through the present reissue application, applicants have submitted new claims 53-63, 65 and 70-74, which are supported by the original disclosure and drawings of the patent. With respect to the new claims, claims 53 and 70 are the independent claims.

Claims 53-63, 65 and 70-74 are supported by Figs. 12A-15C. Figs. 12A-15C are discussed in the specification on pages 9-11 of the specification.

With respect to claim 53, Fig. 15A shows complementary MISFETs including P-channel and N-channel MISFETs T_{33}, T_{32} and a circuit block 61 that also includes an

operating voltage V_{CL2}. In a first operation mode, V_{P1} is at 0 volts. In the second operation mode, V_{BP1} is at -1 volts, as shown in Fig. 15C.

Claim 70 is also supported by Fig. 15A and includes first and second circuit blocks 60, 61. Support for the remainder of the claims is provided by Figs. 12A-15C.

ERROR STATEMENT

Every error in the patent which was corrected in the present reissue application, and which is not covered by any prior declaration submitted in this reissue application, arose without any deceptive intention on the part of the Applicants.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

_____ _____

Date Kiyoo Itoh

_____ _____

Date Yoshinobu Nakagome

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Claim 70 is also supported by Fig. 15A and includes first and second circuit blocks 60, 61. Support for the remainder of the claims is provided by Figs. 12A-15C.

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6/14/2007
Date

Kiyoo Itoh
Kiyoo Itoh

Date

Yoshinobu Nakagome

operating voltage V_{CL2}. In a first operation mode, V_{P1} is at 0 volts. In the second operation mode, V_{BP1} is at -1 volts, as shown in Fig. 15C.

Claim 70 is also supported by Fig. 15A and includes first and second circuit blocks 60, 61. Support for the remainder of the claims is provided by Figs. 12A-15C.

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Date

Kiyoo Itoh

6/18/2007
Date

Yoshinobu Nakagome

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Customer No.	:	24956

CONSENT OF ASSIGNEE TO REISSUE

MAIL STOP: Reissue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The undersigned, assignee of the entire interest in the above-mentioned continuation reissue application and RE37,593 (which matured from parent reissue application 09/095,101, which was a reissue application of original patent no. 5,526,313), hereby consents to the above-mentioned continuation reissue application.

ELPIDA MEMORY, INC.

Jun 12, 2007
Date

Takeo Fujii
Name: Takeo FUJII
Title: Executive Manager
Intellectual Property Gr.
IP & Legal Department

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RIGHT OF ASSIGNEE TO PROSECUTE REISSUE APPLICATION

MAIL STOP: Reissue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The assignee of the entire right, title and interest in and to the invention which is the subject of this reissue application is Elpida Memory, Inc.

A chain of title from the inventors of the patent identified above to the current assignees as follows.

1. From the inventors to Hitachi, Ltd. and

   Hitachi VLSI Engineering Corporation in an assignment dated June 8, 1989.

   This document was recorded in the Patent and trademark Office at Reel 5096,

   Frame 677.

2. From Hitachi VLSI Engineering Corporation to Hitachi ULSI Systems Co., Ltd. by a Change of Name Document dated April 1, 1998, with translation, showing that Hitachi VLSI Engineering Corp. was merged into Hitachi ULSI Systems Co., Ltd. on April 1, 1998. This document was recorded in the Patent and trademark Office at Reel 9605, Frame 0357.

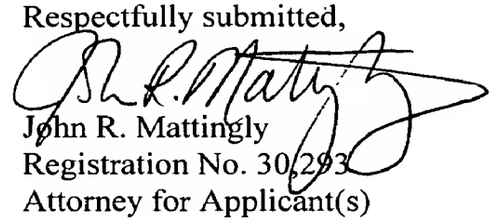
3. From Hitachi ULSI Systems Co., Ltd. and Hitachi, Ltd. to Elpida Memory, Inc. This document was recorded in the Patent and trademark Office at Reel 018563, Frame 0278.

The Assignment documents and Change of Name document noted above establish documentary evidence of a chain of title from the inventors to the current assignee, Elpida Memory, Inc.

AUTHORIZATION TO SIGN STATEMENT

The undersigned attorney is authorized to sign this statement on behalf of the assignee.

Respectfully submitted,



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Date: June 22, 2007